AMENDMENTS TO THE CLAIMS

Cancel claims 1-3, 11-13 and 21-23 without prejudice.

This listing of claims will replace all prior versions, and listings, of claims in the application:

1-3. (canceled)

4. (currently amended) ~~The apparatus of claim 3,~~

An apparatus comprising:

an instruction decoder;

at least one control register coupled to the instruction decoder;

an add-compare-select (ACS) engine coupled to the at least one control register, said ACS engine including:

a plurality of ACS units to perform ACS operations;

a branch metric register coupled to the ACS units to supply branch metric data to the ACS units; and

a plurality of accumulators coupled to the ACS units to store results of the ACS operations performed by the ACS units; and

a memory coupled to the ACS units, to the branch metric register, and to the accumulators;

wherein the instruction decoder is operative to control the ACS engine to perform a first Viterbi decoding mode in response to the instruction decoder receiving a first instruction, the instruction decoder is further operative to control the ACS engine to perform a second Viterbi

decoding mode different from the first Viterbi decoding mode in response to the instruction decoder receiving a second instruction, and the instruction decoder is further operative to control the ACS engine to perform turbo decoding in response to the instruction decoder receiving a third instruction; and

wherein in ~~a~~ the first Viterbi decoding mode ~~of operating the apparatus operands~~ path metrics are ~~supplied to the ACS units~~ updated from the accumulators and in ~~a~~ the second Viterbi decoding mode ~~of operating the apparatus operands~~ path metrics are ~~supplied to the ACS units~~ updated from the memory.

5. (currently amended) The apparatus of claim ~~2~~ 4, wherein the plurality of accumulators includes four accumulators.

6. (original) The apparatus of claim 5, wherein each of the accumulators includes eight units, each unit being capable of storing 48 bits.

7. (original) The apparatus of claim 6, wherein the 48 bits stored in each accumulator unit include 16 guard bits.

8. (currently amended) The apparatus of claim ~~2~~ 4, wherein each of the ACS units is capable of performing butterfly operations.

9. (original) The apparatus of claim 8, wherein:

a final add of a butterfly operation performed by one of the ACS units is a two-operand add if the ACS engine is performing Viterbi decoding; and

the final add of the butterfly operation is a three-operand add if (a) the ACS engine is performing turbo decoding and (b) a certain intermediate result is obtained during the final add.

10. (original) The apparatus of claim 9, wherein an operand for the three-operand add is looked up in a look up table if (a) the ACS engine is performing turbo decoding and (b) the certain intermediate result is obtained during the final add.

11-13. (canceled)

14. (currently amended) ~~The system of claim 13,~~

A system comprising:

a forward error correction decoder; and

a speaker coupled to the forward error correction decoder to audibly reproduce corrected data output from the forward error correction decoder;

wherein the forward error correction decoder includes:

an instruction decoder;

at least one control register coupled to the instruction decoder;

an add-compare-select (ACS) engine coupled to the at least one control register, said ACS engine including:

a plurality of ACS units to perform ACS operations;

a branch metric register coupled to the ACS units to supply branch metric data to the ACS units; and

a plurality of accumulators coupled to the ACS units to store results of the ACS operations performed by the ACS units; and

a memory coupled to the ACS units, to the branch metric register, and to the accumulators;

wherein the instruction decoder is operative to control the ACS engine to perform a first Viterbi decoding mode in response to the instruction decoder receiving a first instruction, the instruction decoder is further operative to control the ACS engine to perform a second Viterbi decoding mode different from the first Viterbi decoding mode in response to the instruction decoder receiving a second instruction, and the instruction decoder is further operative to control the ACS engine to perform turbo decoding in response to the instruction decoder receiving a third instruction; and

wherein in ~~a~~ the first Viterbi decoding mode ~~of operating the system operands~~ path metrics are ~~supplied to the ACS units~~ updated from the accumulators and in ~~a~~ the second Viterbi decoding mode ~~of operating the system operands~~ path metrics are ~~supplied to the ACS units~~ updated from the memory.

15. (currently amended) The system of claim ~~12~~ 14, wherein the plurality of accumulators includes four accumulators.

16. (original) The system of claim 15, wherein each of the accumulators includes eight units, each unit being capable of storing 48 bits.

17. (original) The system of claim 16, wherein the 48 bits stored in each accumulator unit include 16 guard bits.

18. (currently amended) The system of claim ~~12~~ 14, wherein each of the ACS units is capable of performing butterfly operations.

19. (original) The system of claim 18, wherein:

a final add of a butterfly operation performed by one of the ACS units is a two-operand add if the ACS engine is performing Viterbi decoding; and

the final add of the butterfly operation is a three-operand add if (a) the ACS engine is performing turbo decoding and (b) a certain intermediate result is obtained during the final add.

20. (original) The system of claim 19, wherein an operand for the three-operand add is looked up in a look up table if (a) the ACS engine is performing turbo decoding and (b) the certain intermediate result is obtained during the final add.

21-23. (canceled)